High-Performance USB PD3.0/PPS/QC4/4+ Controller

Description

The CY2332 is a highly integrated USB Type-C power delivery controller and targeted for USB-Type-C adapter and charger application. It has passed USB-IF certifications of USB power delivery specification Rev 3.0 V1.2 with PPS. Also, CY2332 is compatible with Qualcomm QC4/4+ protocol.

The CY2332 can support PPS APDO (Augmented Power Data Object) with 20mV/step voltage resolution and 50mA/step current resolution for power management. What's more, cable-loss compensation and SOP' command for e-Marker detection are embedded too. Also, CY2332 drives external NMOS for VBUS on/off switch.

The CY2332 can provide robust protection scheme with built-in OVP/OCP/SCP features. There are rich power functions embedded on the chip so as to reduce total BOM. An one-time–programmable ROM is provided for main firmware, and multi-time-programmable ROM is provided for user configuration data.

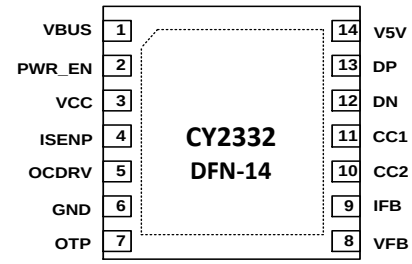
Features

- Compatible with USB PD Rev 3.0 V1.2
- USB-IF PD3.0/PPS Certificated TID = 78
- Qualcomm QC4/4+ Protocol supported
- OTP (One-Time-Programmable) for Main Firmware
- MTP (Multi-Time-Programmable) for System Configuration
- Built-In Regulator for CV and CC Control
- Support SCP/OVP/UVP with Auto Restart
- Support Power Saving Mode
- External N-MOSFET Control for VBUS Power Delivery
- Support e-Marker Cable Detection
- Operating Voltage Range: 3.3V to 20V
- I2C Interface and GPIOs Supported (QFN-24 & TSSOP-16)
- Fewest External Component Counts
- Totally Lead-Free & Fully RoHS Compliant (Note 1)
- Halogen and Antimony Free. "Green" Device (Note 2)

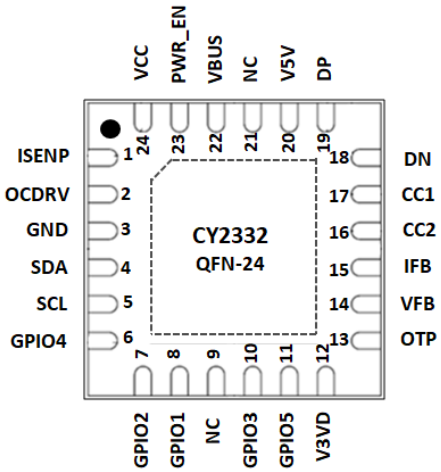
Applications

- Type-C USB Adapter/Charger
- USB PD Converter

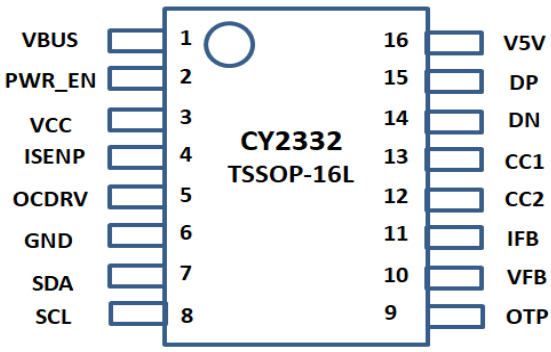
Pin Assignments



W-DFN3030-14



W-QFN4040-24



TSSOP173-16

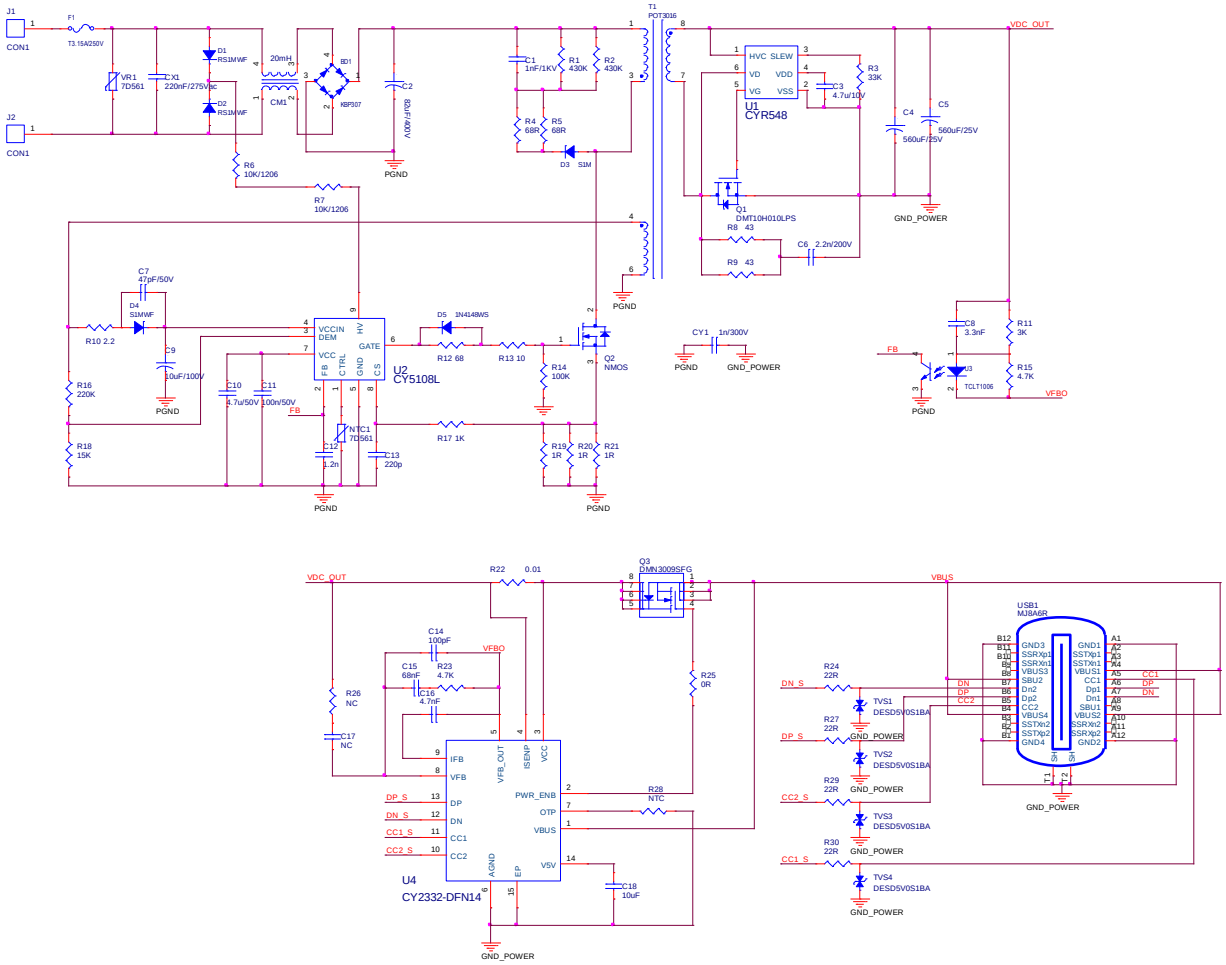
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

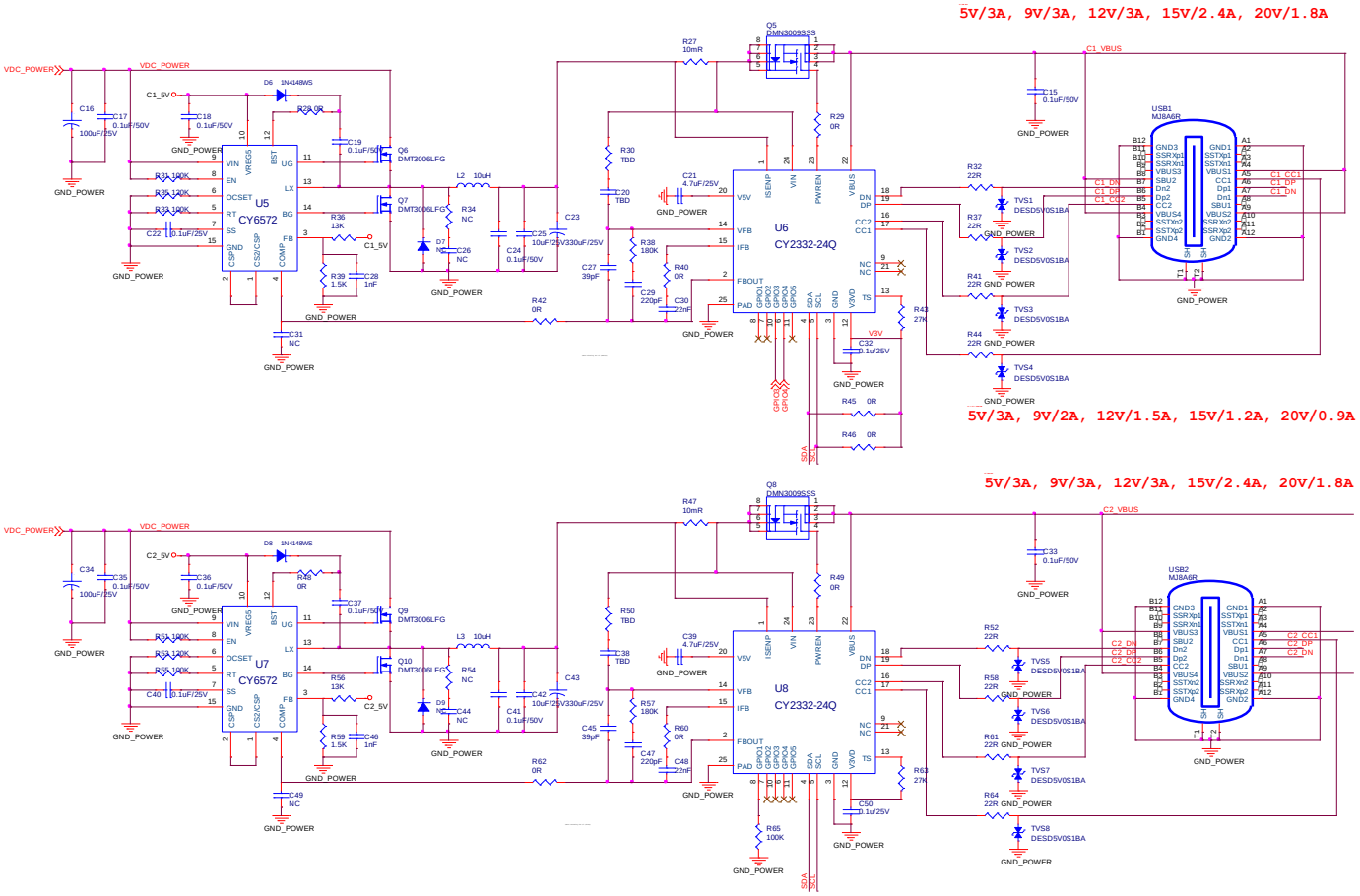
Case 1: 1C Port Application with CY2332 DFN-14

High Performance and low cost USB PD adapter is implemented through CY2332 DFN-14 protocol controller and some power chips.



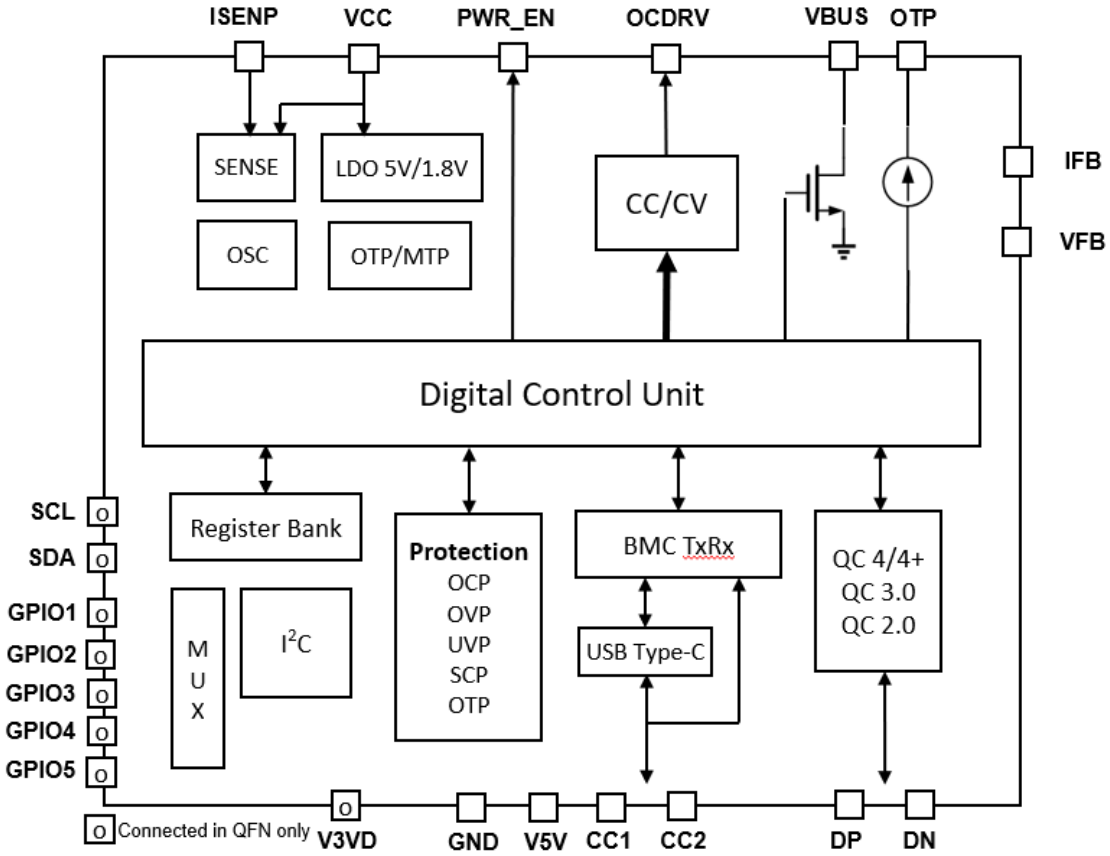
Case 2: 2C Port Application with CY2332 QFN-24

Smart power sharing is implemented through I2C communication between master CY2332 and slave CY2332. CY2332 QFN-24 not only includes CY2332 DFN-14 functions, but also supports I2C master/slave interfaces and 5 GPIOs. It is a good candidate for smart multi-port power adapter applications.



Functional Block Diagram

CY2332 includes full features of PD protocol controller. For compact application, DFN-14 package is supported. For smart power sharing and multi-port applications, QFN-24 is used to connect out all of the pins, including I2C and 5 GPIOs. For wider pitch in manufacture, TSSOP-16 is supported with I2C capability.



Pin Descriptions

DFN-14 Pin No	QFN-24 Pin No	TSSOP-16 Pin No.	Pin Name	Pin Function
1	22	1	VBUS	Output Terminal for Discharge Path.
2	23	2	PWR_EN	External NMOS Gate Driver. To control External MOS switch: 1: Enable VBUS voltage, 0: Disconnect VBUS.
3	24	3	VCC	The power supply of the IC, connected to a ceramic capacitor.
4	1	4	ISENP	Input Current Sense Positive Node.
5	2	5	OCDRV	CC/CV Output. Open Drain Output for Opto-Coupler.
6	3	6	GND	Ground
7	13	9	OTP	Source current to external NTC sensor for OTP (Over Temperature Protection).
8	14	10	VFB	CV Input. Negative Node of CV OPAMP for Opto-Coupler.
9	15	11	IFB	CC Input. Negative Node of CC OPAMP for Opto-Coupler.
10	16	12	CC2	Type-C_CC2
11	17	13	CC1	Type-C_CC1
12	18	14	DN	Type-C_DN
13	19	15	DP	Type-C_DP
14	20	16	V5V	LDO-5V Output
-	4	7	SDA	GPIO/I2C Data
-	5	8	SCL	GPIO/I2C Clock
-	6		GPIO4	General Purpose Input/Output
-	7		GPIO2	General Purpose Input/Output
-	8		GPIO1	General Purpose Input/Output
-	9		NC	No Connection
-	10		GPIO3	General Purpose Input/Output
-	11		GPIO5	General Purpose Input/Output
-	12		V3VD	LDO-3V Output
-	21		NC	No Connection

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{VCC}	Input Voltage at VCC Pin	-0.3 to 24	V
V_{VFB}, V_{IFB}, V_{OTP}	Input Voltage at VFB, IFB, OTP Pins	-0.3 to 7	V
V_{VBUS}, V_{ISENP}, V_{OCDRV}	Input Voltage at VBUS, ISENP, OCDRV Pins	-0.3 to 24	V
V_{PWR_EN}	Input Voltage at PWR_EN Pin	-0.3 to 24	V
V_{V5V}	Input Voltage at V5V Pin	-0.3 to 7	V
V_{CC1}, V_{CC2}	Input Voltage at CC1, CC2 Pins	-0.3 to 7	V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	-0.3 to 7	V
V_{V3VD}	Input Voltage at V3VD Pin	-0.3 to 5	V
V_{GPIO1} - V_{GPIO5}, V_{SDA}, V_{SCL}	Input Voltage at GPIO1 - GPIO5, SDA, SCL Pins	-0.3 to 5	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	122	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 5)	27	°C/W
—	ESD (Human Body Model) Voltage on DP, DN Pins	8	kV
—	ESD (Human Body Model) Voltage on Other Pins	2	kV
—	ESD (Charged Device Model)	750	V

Note: 4. Stresses greater than those listed under "*Absolute Maximum Ratings*" can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "*Recommended Operating Conditions*" is not implied. Exposure to "*Absolute Maximum Ratings*" for extended periods can affect device reliability.
5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{VCC}	Input Voltage at VCC Pin	3.3	21	V
V_{GPIO1} - V_{GPIO5}, V_{SDA}, V_{SCL}	Input Voltage at GPIO1 - GPIO5, SDA, SCL Pins	0	3.7	V
T_{OP}	Operating Temperature Range	-40	+85	°C

Electrical Characteristics ($@T_A$ = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC PIN SECTION						
V_{ST}	Startup Voltage	—	2.7	2.8	3.2	V
V_{UVLO}	Minimum Operating Voltage	—	2.6	2.7	3	V
V_{CC_HYS}	V_{CC} Hysteresis (V_{ST}-V_{UVLO})	—	0.1	-	-	V
$I_{CC\_DEEP\ SLEEP}$	V_{IN} Current in Deep Sleep Mode	CC1/2 Detach after 3s	-	550	660	A
I_{CC_OPR}	Operating Supply Current	—	-	3.3	6	mA
LDO Output						
V_{V5V}	LDO Output	—	4.4	5	5.5	V
V_{V3VD}	LDO Output		-	3	-	V
VOLTAGE CONTROL LOOP SECTION						
V_{REF_CV5}	Reference Voltage for 5V CV Control	—	4.85	5.0	5.15	V
V_{REF_CV9}	Reference Voltage for 9V CV Control	—	8.73	9.0	9.27	V
V_{REF_CV12}	Reference Voltage for 12V CV Control	—	11.64	12.0	12.36	V
V_{REF_CV20}	Reference Voltage for 20V CV Control	—	19.4	20	20.6	V
V_{CABLE}	Cable Compensation (Note 6)	—	24	30	36	mV/A
I_{OS}	Maximum OCDRV Pin Sink Current	V_{OUT} = 5V	10	16	30	mA
PROTECTION FUNCTION SECTION						
V_{OVP5V}	OVP_5V Enable Voltage (Note 7)	—	5.5	6	7.0	V
V_{OVP9V}	OVP_9V Enable Voltage (Note 7)	—	9.9	10.8	12.1	V
V_{OVP12V}	OVP_12V Enable Voltage (Note 7)	—	13.2	14.4	16.2	V
V_{OVP20V}	OVP_20V Enable Voltage (Note 7)	—	-	24	-	V
$t_{DEBOUNCE\_OVP}$	OVP Debounce Time (Note 9)	—	-	90	-	ms
V_{UVP5V}	UVP_5V Enable Voltage	—	3.3	3.8	4.1	V
V_{UVP9V}	UVP_9V Enable Voltage	—	5.9	7.2	7.7	V
V_{UVP12V}	UVP_12V Enable Voltage	—	8.5	9.1	9.8	V
V_{UVP20V}	UVP_20V Enable Voltage	—	-	15	-	V
I_{OVD}	Over Voltage Discharge Current	—	-	240	-	mA
t_{OCP}	OCP Deglitch Time (Note 8)	—	-	30	-	ms
$t_{RESTART\_INTERVAL\_SCP}$	Restart Interval Time under SCP (Note 8)	—	1	-	2	s
$I_{OTP\_EXTERNAL}$	External OTP Current	—	-	100	-	A

Notes: 6. Cable compensation voltage can be adjusted by setting from 0 to V_{CABLE} * N, (N: 0 to 7).
7. 120% OVP setting.
8. Guaranteed by design.
9. OVP blanking time during V_O transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.

Electrical Characteristics (@T_A =+25°C, V_{VCC} = 15V, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PROTECTION FUNCTION SECTION						
t_{SLEEP}	Enter Sleep Mode Time after Cable Detached (Note 8)	—	-	3	-	s
t_{OV_DELAY}	Delay from OVP Threshold Trip to NMOS Gate Turn-Off (Note 8)	—	-	-	50	μs
t_{UV_DELAY}	Delay from UVP Threshold Trip to NMOS Gate Turn-Off (Note 8)	—	-	-	50	μs
CC1/CC2，DP/DN SECTION						
V_{L_RD3A}	Low Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	-	1.35	-	V
V_{H_RD3A}	High Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	-	2.0	-	V
I_{RD3A}	CC1/CC2 Current Source for 3A Advertisement	—	304	330	356	μA
V_{OVP_DN}	DN Line Over Voltage Protection Threshold	—	4.2	4.5	4.8	V
V_{OVP_DP}	DP Line Over Voltage Protection Threshold	—	4.2	4.5	4.8	V

Note: 8. Guaranteed by design.

Performance Characteristics

System Power-On Sequence:
When the external power source is provided, the CY2332 will wake up, and the USB PD controller and MCU will be initialized. All analog control blocks are ready and waiting for PD negotiation process. Meanwhile, the CY2332 monitors the voltage and current conditions to avoid abnormal conditions happen. Once any unacceptable condition happens, the CY2332 will go into protection procedure according to the types of abnormal conditions happen.

Voltage Transition
According to USB PD's protocol, the PD device requests different power profile and the CY2332's power control blocks will change voltage and current values. The CY2332 provides corresponding Over Voltage Protection (OVP), Over Current Protection (OCP) scheme, and feedback system stability to guarantee monotonic voltage transition and avoid violating USB PD electrical specification.

The CY2332 provides zero-mismatch voltage methodology that is more flexible for customer system design requirement. When UFP/DFP makes an acceptable power request deal, the CY2332 will change the VFB pin voltage according to the USB PD command. The voltage regulator control loop regulates the required V_{BUS} voltage according to V_{FB}. In addition, the shunt regulator is built in to minimize the total external components and cost.

Protection
The CY2332 provides OVP/UVP/OCP/SCP functions and also support Constant Current (CC) function. All of the protection thresholds depend on the requested power profile, and provide the most reliable protection scheme.

The CY2332 provides OVP feature by turning off the power switch when V_{BUS} is higher than OVP enable voltage. Meanwhile, it provides internal discharge path to reduce the overvoltage duration, and terminates discharge current as soon as V_{BUS} reaches the target voltage. To avoid the VBUS pin working abnormally, the CY2332 provides UVP function whenever V_{BUS} drops to UVP enable voltage.

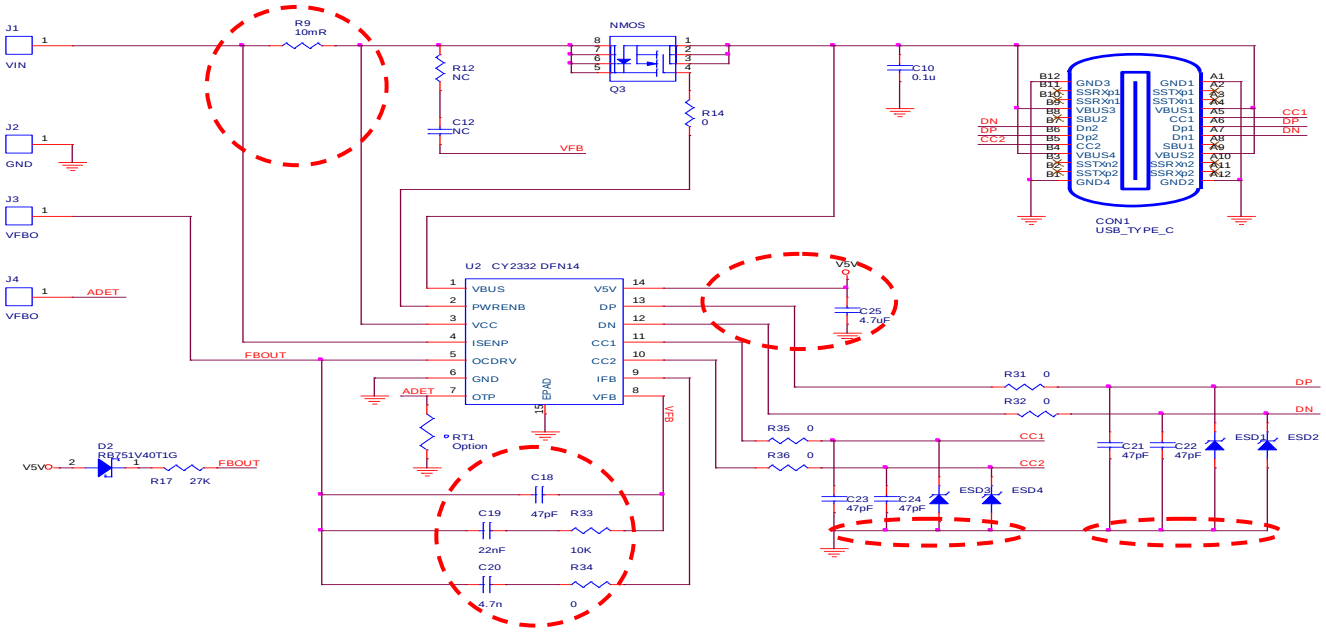
To ensure the safe operation of USB PD, the CY2332 provides programmable OCP function to make sure output current will not be higher than the allowed maximum current. Once OCP conditions happen, the CY2332 will shut down the USB PD system and send "Hard Reset" to the Upstream-Facing Port (UFP) device.

CV/CC
The CY2332 supports Constant Voltage (CV) and Constant Current (CC) functions to control the output voltage and the output current by the control pin OCDRV. During the CV mode, the CY2332 operates in fixed PDO, and the output voltage will be regulated to the request voltage if the output current is below the allowed maximum current. Once the sink device draws more than I_{OCP}, the over current protection occurs. When the CC mode function is enabled, the output voltage drops, and the source current is limited within 150mA whenever output current exceeds the allowed maximum current. When the output voltage drops below UVP, constant current limit turns off V_{BUS} and starts error recovery procedure. The CY2332 will reset if the voltage continues dropping to UVLO threshold.

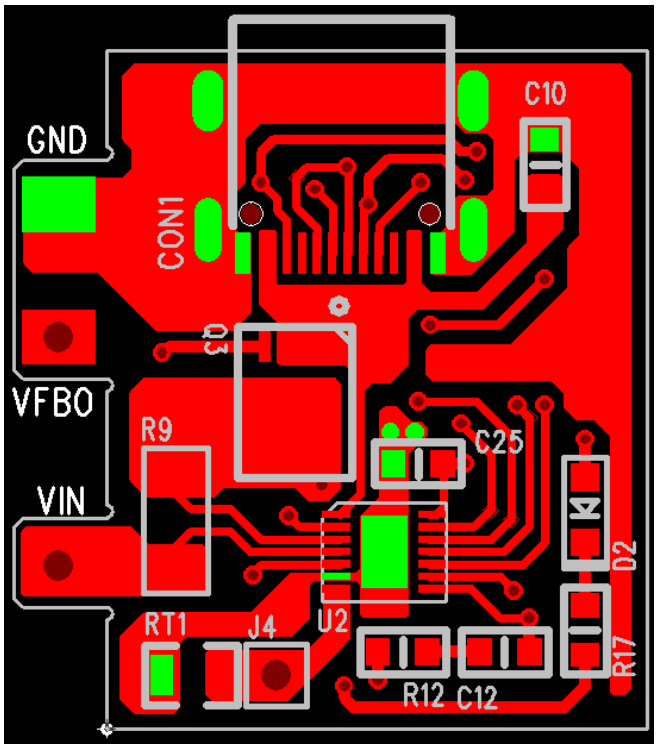
I2C Interface
The CY2332 supports I2C Interface with Slave and Master modes in QFN-24 and TSSOP-16 packages. By default it is slave mode. The I2C peripherals are compatible with the I2C Standard-mode, Fast-mode, and Fast-mode Plus devices. The I2C bus I/Os are implemented with GPIO in open-drain modes.

PCB Layout Guidelines

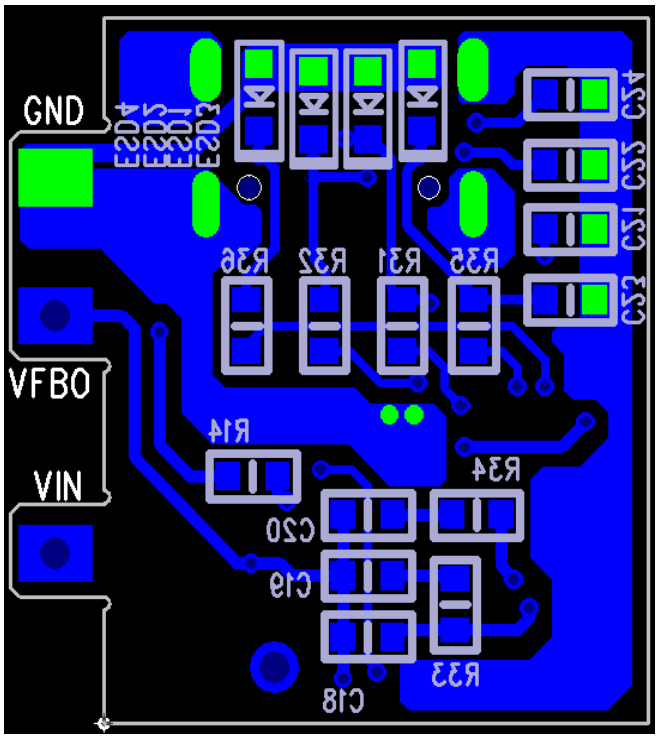
CY2332 performance is dramatically affected by its PCB layout. It is recommended to follow these general guidelines show below. For simplicity, the guidelines are illustrated based on a real PCB layout of a typical CY2332 DFN-14 application circuit as below:



TOP

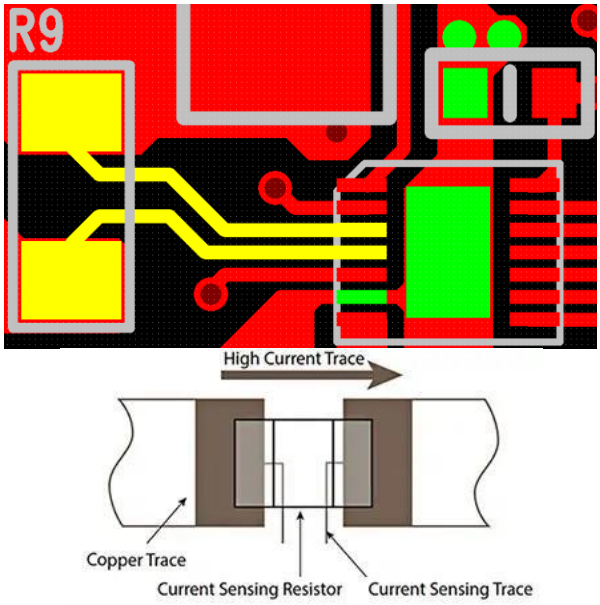


BOTTOM



1. Current Sense Resistor (R9)

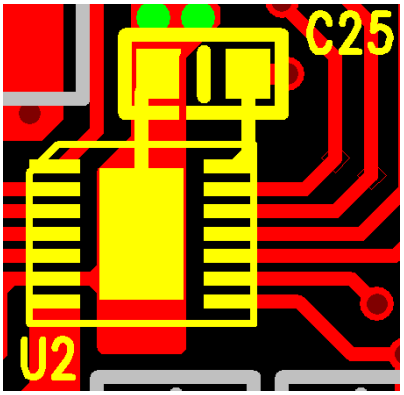
Use 4-points Kelvin connections to current sense resistor. Current sense signals, Pin 3(VCC) and Pin 4(ISENP), should be connected to R9 in parallel, equal length, and reduce the distance if possible.



2. V5V Decoupling Capacitor (C25) and GND

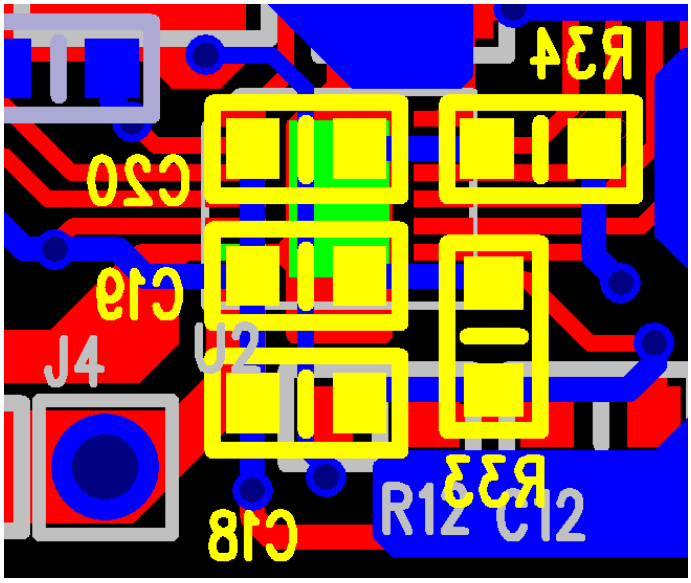
Keep C25 closed enough to IC V5V(PIN14)。

C25 is used to regulate and decouple the output of internal LDO, V5V. GND(PIN6) is suggested to return to C25 cathode directly and independently, and to avoid the connection with any high current point to reduce the interference accordingly.



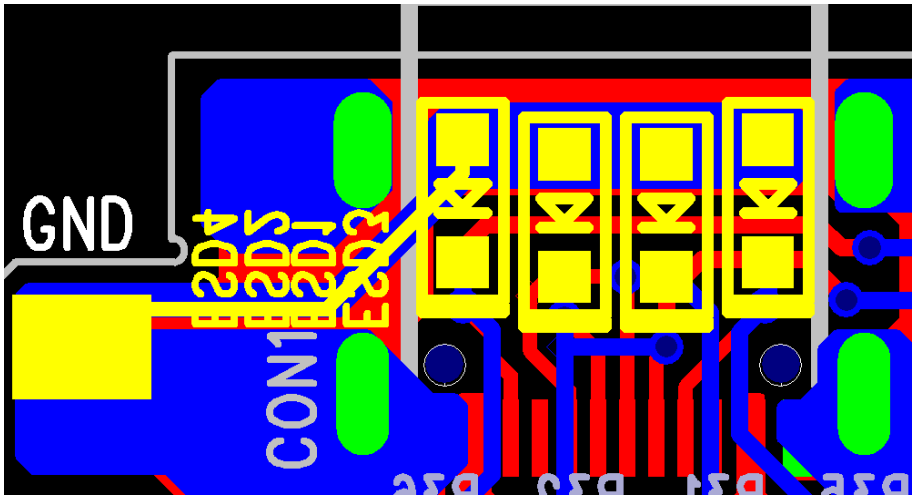
3. CV/CC Compensation Loop

Any high current or high frequency routes are prohibited to cross or close to the area of CC/CV compensation components: C18, C19, C20, R33, R34. Also, CC/CV compensation components should be closed to CY2332 Pin8 (VFB),,Pin9 (IFB), and Pin5 (OCDRV).



4. ESD Protection Placement

The GND for ESD protection devices are suggested to go back to Cin cathode, or GND connection of the small PD module. In general, ESD protection devices are put on CC1/CC2 and DP/DN of the type-C connector. Any high voltage or current induced by ESD event will go back to Cin cathode directly. Otherwise, it will enter into CY2332 and its peripheral devices to cause damage.



For the detail of CY2332 layout guide, please refer to Application Note ***AN2001.***

Ordering Information

Part Number	Package Type	Package Outline	MOQ	Shipping Support
CY2332FBZ-13	W-DFN-14	3mm*3mm	3000	Tape / Reel
CY2332FBZ-13-05	W-DFN-14	3mm*3mm	3000	Tape / Reel
CY2332-24Q	W-QFN-24	4mm*4mm	3000	Tape / Reel
CY2332-16L	TSSOP-16	173 mil	3000	Tape / Reel

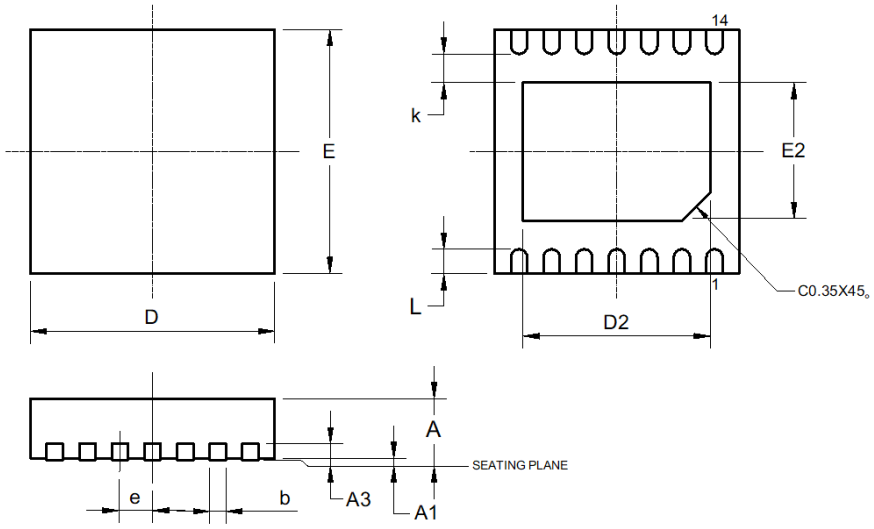
IC Marking

(Top View)

2332	Device Name
YYWW	YearWeek
ZZ	Internal Code

Package Outline Dimensions

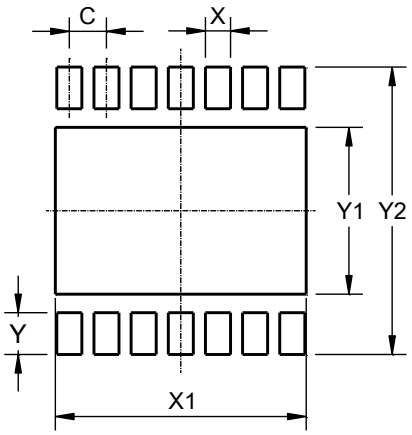
– **W-DFN3030-14**



W-DFN3030-14 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0	0.05	0.02
A3	0.203REF		
b	0.15	0.25	0.20
D	3.00BSC		
D2	2.55	2.65	2.60
e	0.40BSC		
E	3.00BSC		
E2	1.65	1.75	1.70
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

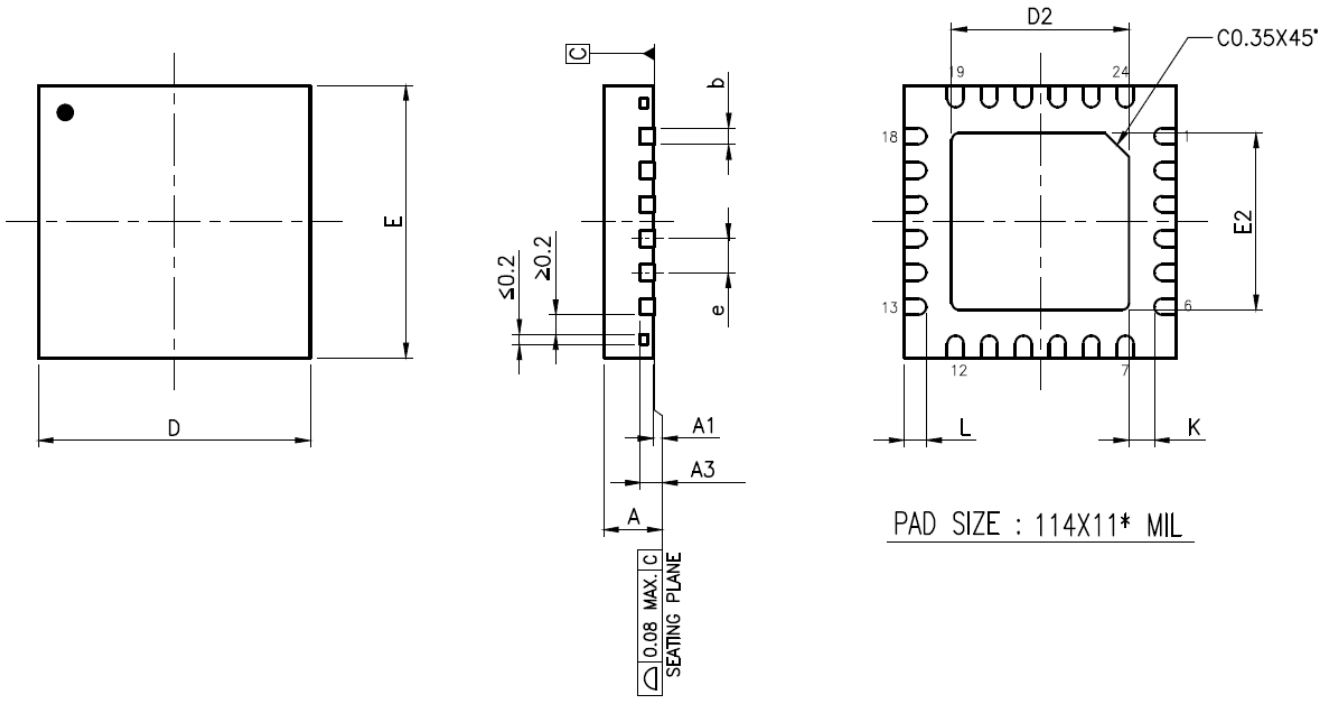
Please see http://www.canyon-semi.com.tw/package-outlines.html for the latest version.



Dimensions	Value (in mm)
C	0.40
X	0.27
X1	2.70
Y	0.45
Y1	1.80
Y2	3.10

Package Outline Dimensions

– W-QFN4040-24

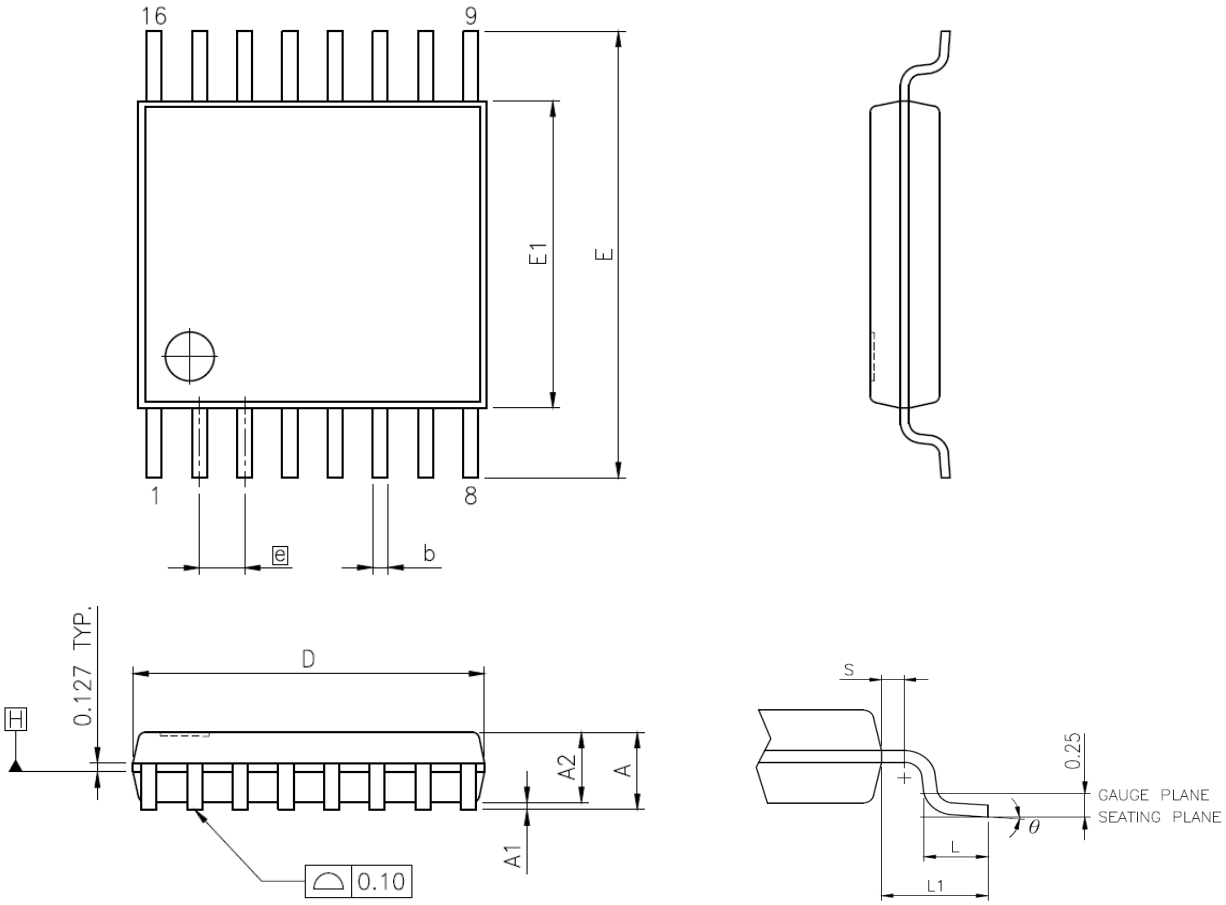


	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X424)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
K	0.20	—	—

PAD SIZE	b			D2			E2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
114X11* MIL	0.18	0.25	0.30	2.65	2.70	2.75	2.65	2.70	2.75	0.35	0.40	0.45	V	X	W(V)GGD-6

Package Outline Dimensions

– **TSSOP173-16**



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS		MIN.	NOM.	MAX.
A		—	—	1.20
A1	STANDARD	0.05	—	0.15
⑥	THERMALLY ENHANCED	0.00	—	0.15
A2		0.80	1.00	1.05
b		0.19	—	0.30
D		4.90	5.00	5.10
E1		4.30	4.40	4.50
E			6.40 BSC	
e			0.65 BSC	
L1			1.00 REF	
L		0.45	0.60	0.75
S		0.20	—	—
θ		0°	—	8°

Revision History

Revision	Comment	Issue Date	Author
0.1	Initial Release	05/30/2019	William Yang
0.5	W-QFN4040-24 Package is added	10/28/2019	William Yang
2.1	Update A1 and A3 in POD of W-DFN3030-14	03/06/2024	William Yang