Canyon Semiconductor Inc.

Lead-free Green

# CY2569
# USB PD SINK CONTROLLER

## Description

The CY2569, a highly integrated USB Type-C PD3.0/PPS sink controller, is targeted for DC power request and control for a Type-C Connector equipped Devices (TCD). To leveraging increasing popularity of standard Type-C PD3.0 power adaptors, the CY2569 negotiates with an existing PD3.0 adaptor to acquire the required power profile to supply the TCD.

Working its role as DC-Power request from a USB PD source, the CY2569 interprets power input requirements (voltage/current and maximum power) from the TCD, and then establishes power link through configuration channel (CC) communication with an external USB PD3.0 adaptor to output a suitable DC power for TCD device. The voltage requests could be easily specified by 3 pins (VSEL2, VSEL1, VSEL0), up to 8 voltages can be selected and both fixed PDO (Power Data Object) and PPS APDO (Augmented Power Data Object) in PD source adapter are supported in CY2569 search algorithm. Also, up to 10 maximum power levels can be selected through different resistance value of the resistor connected to pin PSEL (refer to figure 1 and 2).

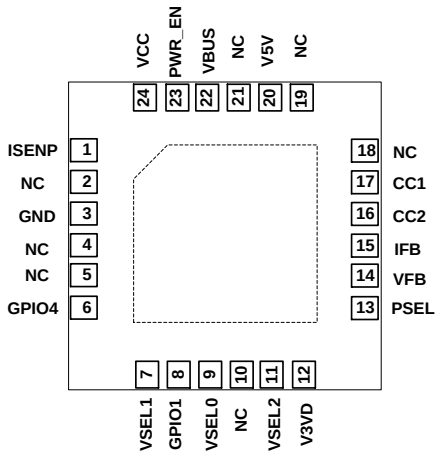
There are rich power functions embedded as hardware or enabled by built-in firmware in the chip so as to reduce total BOM while maintain maximum flexibility. A one-time–programming (OTP) ROM is provided to store the PD/Sink controller firmware.

## Features

- Compliant with USB PD Rev 3.0 v1.2
- USB-IF certificated TID: 5000
- Ease of use without any firmware programming
- Up to 8 Voltage selections by 3-pin setting
- Support dynamic pin setting with periodic scanning
- Up to 10 Power selections by 1-pin attached resistor
- Support OVP with hard reset and auto restart
- Support Driver for N-MOS VBUS Power Switch
- Support Dead-battery mode
- Support LED indication of charging and fault status
- Operating Voltage Range: 3.3V to 24V
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)

## Pin Assignments

**(Top View)**




**W-QFN4040-24 (Type A1)**

## Applications

- Type-C Connector Equipped Battery-Powered Devices
- Type-C Connector Equipped DC-Power Input Devices
- Type-C-to-Traditional Barrel Connector Power Adaptor Cables

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. Contact http://www.canyon-semi.com.tw for more information of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Typical Applications Circuit

The CY2569 is an USB Type-C power delivery sink controller and used to request a specific power profile from a standard USB PD 3.0 compliance source adapter, as shown in the figure below.

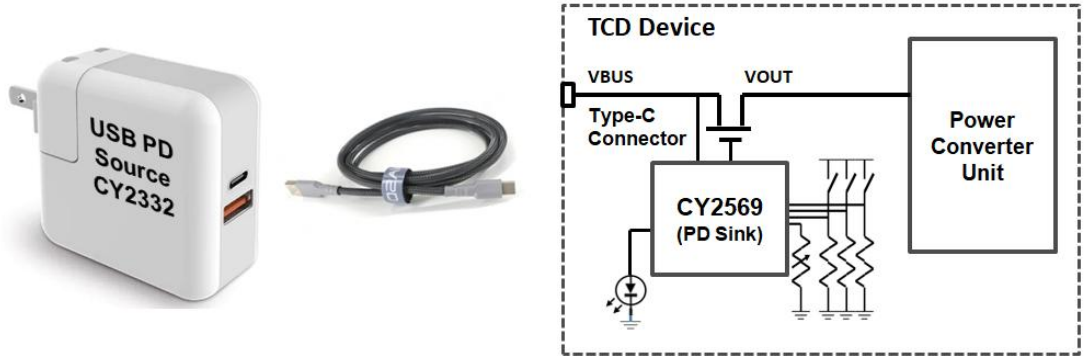
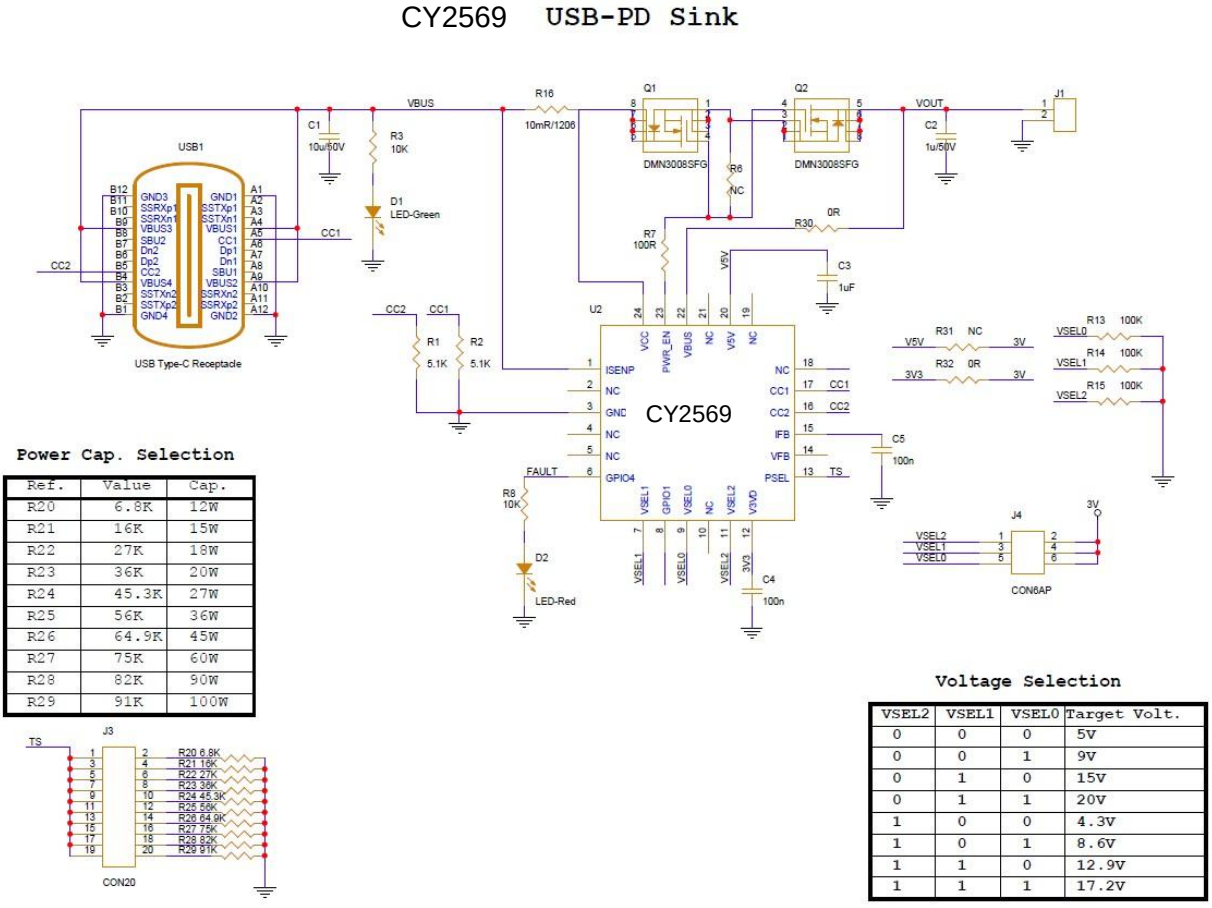



**Figure 1. Typical Application structure of CY2569**

The CY2569 can request a power through resistor setting. A typical setting of CY2569 to get a DC power is shown as below.




**Power Cap. Selection**

| Ref. | Value | Cap. |
|---|---|---|
| R20 | 6.8K | 12W |
| R21 | 16K | 15W |
| R22 | 27K | 18W |
| R23 | 36K | 20W |
| R24 | 45.3K | 27W |
| R25 | 56K | 36W |
| R26 | 64.9K | 45W |
| R27 | 75K | 60W |
| R28 | 82K | 90W |
| R29 | 91K | 100W |

**Voltage Selection**

| VSEL2 | VSEL1 | VSEL0 | Target Volt. |
|---|---|---|---|
| 0 | 0 | 0 | 5V |
| 0 | 0 | 1 | 9V |
| 0 | 1 | 0 | 15V |
| 0 | 1 | 1 | 20V |
| 1 | 0 | 0 | 4.3V |
| 1 | 0 | 1 | 8.6V |
| 1 | 1 | 0 | 12.9V |
| 1 | 1 | 1 | 17.2V |

**Figure 2. Typical Application Circuit of CY2569**

## Pin Descriptions

| Pin No | Pin Name | Type (Note) | Pin Function |
|---|---|---|---|
| 1 | ISENP | AIO | Current Sense Positive Node. |
| 2 | NC | - | No Connection |
| 3 | GND | GND | Ground |
| 4 | NC | - | No Connection |
| 5 | NC | - | No Connection |
| 6 | GPIO4 | DIO | General Purpose Input/Output pin, for LED usage. |
| 7 | VSEL1 | DIO | For Voltage Select Pin1 |
| 8 | GPIO1 | DIO | General Purpose Input / Output |
| 9 | VSEL0 | DIO | For Voltage Select Pin0 |
| 10 | NC | - | No Connection |
| 11 | VSEL2 | DIO | For Voltage Select Pin2 |
| 12 | V3VD | DP | 3.3V LDO Output.<br>Power for Digital circuit and Digital I/O pins, with 0.1uF to Ground |
| 13 | PSEL | AIO | For Power Capability Selection. |
| 14 | VFB | AI | For Voltage Measurement. |
| 15 | IFB | AI | For Current Measurement, with 100nF to Ground |
| 16 | CC2 | AIO | Type-C configuration channel 2 |
| 17 | CC1 | AIO | Type-C configuration channel 1 |
| 18 | NC | - | No Connection |
| 19 | NC | - | No Connection |
| 20 | V5V | AP | 5V LDO output.<br>Power for Analog circuit and Analog I/O pins, with 1uF to Ground |
| 21 | NC | - | No Connection |
| 22 | VBUS | AHV | Terminal for Discharge Path. |
| 23 | PWR_EN | AHV | To control external NMOS switch ON (High) or OFF (Low). |
| 24 | VCC | AHV | The power supply of the IC, connected to a ceramic capacitor. |
| - | EP | GND | Exposed pad is connected to Ground |

Note:
AHV– Analog High Voltage pin
AP – Power for Analog Circuit and Analog I/O pins, 5.0V operation
AI – Analog Input pin
DP – Power for Digital Circuit and I/O pins, 3.3V operation
AIO – Analog I/O pin.
DIO – Digital I/O pin.

## Functional Block Diagram

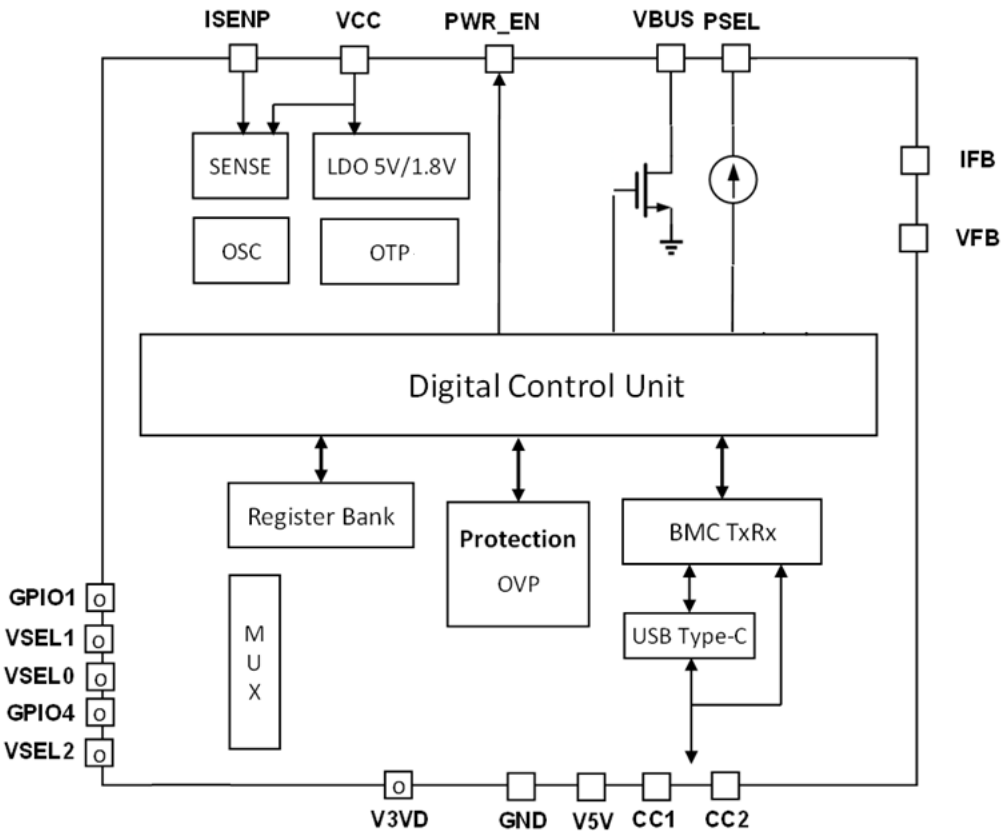



**Figure 3. Functional Block Diagram of CY2569**

## Absolute Maximum Ratings (Note 4)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{VCC}$ | Input Voltage at VCC Pin | -0.3 to 24 | V |
| $V_{FB}$, $V_{IFB}$, $V_{PSEL}$ | Input Voltage at VFB, IFB, PSEL Pins | -0.3 to 7 | V |
| $V_{VBUS}$, $V_{PWR\_EN}$, $V_{ISENP}$ | Input Voltage at VBUS, PWR_EN, ISENP Pins | -0.3 to 24 | V |
| — | Voltage from PWR_EN to VCC Pin | -16 to 7 | V |
| $V_{V5V}$ | Input Voltage at V5V Pin | -0.3 to 7 | V |
| $V_{V3VD}$ | Input Voltage at V3VD Pin | -0.3 to 5 | V |
| $V_{CC1}$, $V_{CC2}$ | Input Voltage at CC1, CC2 Pins | -0.3 to 7 | V |
| $V_{GPIO1}$, $V_{GPIO4}$, $V_{VSEL0}$ – $V_{VSEL2}$ | Input Voltage at GPIO1, GPIO4, VSEL0 – VSEL2 Pins | -0.3 to 5 | V |
| $T_J$ | Operating Junction Temperature | -40 to +150 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $T_{LEAD}$ | Lead Temperature (Soldering, 10s) | +300 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction to Ambient) (Note 5) | 28 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction to Case) (Note 5) | 16 | °C/W |
| ESD | Human Body Model | 2 | kV |
| ESD | Charged Device Model | 750 | V |

Notes: 4. Stresses greater than those listed under "*Absolute Maximum Ratings*" can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "*Recommended Operating Conditions*" is not implied. Exposure to "*Absolute Maximum Ratings*" for extended periods can affect device reliability.
5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

## Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{VCC}$ | Power Supply Voltage | 3.3 | 24 | V |
| $V_{VSEL0}$ ~ $V_{VSEL2}$ | Input Voltage at VSEL0 ~ VSEL2 Pins | 0 | 3.7 | V |
| $V_{GPIO1}$, $V_{GPIO4}$, | Input Voltage at GPIO1, GPIO4 Pins | 0 | 3.7 | V |
| $T_{OP}$ | Operating Temperature Range | -40 | +85 | °C |

## Electrical Characteristics (@ $T_A$ = +25°C, unless otherwise specified.)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VCC SECTION** | | | | | | |
| $V_{ST}$ | Startup Voltage | — | 2.5 | 2.8 | 3.2 | V |
| $V_{UVLO}$ | Minimum Operating Voltage | — | 2.4 | 2.7 | 3 | V |
| $V_{VCC\_HYS}$ | $V_{CC}$ Hysteresis ( $V_{ST}$-$V_{UVLO}$ ) | — | 0.05 | — | — | V |
| $I_{VCC\_OPR}$ | Operating Supply Current | $V_{CC}$ = 5V | — | 3.3 | 6 | mA |
| **CC1/CC2 SECTION** | | | | | | |
| $V_{L\_RD3A}$ | Low Voltage Threshold Used to Distinguish $R_D$ Attached or Detached for 3A Delivery | — | — | 1.35 | — | V |
| $V_{H\_RD3A}$ | High Voltage Threshold Used to Distinguish $R_D$ Attached or Detached for 3A Delivery | — | — | 2.0 | — | V |
| **VOLTAGE SELECTION AND POWER SELECTION** | | | | | | |
| $V_{VSEL\_HI}$ | VSEL0 ~ VSEL2 High Voltage (Note 7) | $V_{CC}$ = 5V | 1.4 | | | V |
| $V_{VSEL\_LO}$ | VSEL0 ~ VSEL2 Low Voltage (Note 7) | $V_{CC}$ = 5V | | | 0.4 | V |
| $T_{VSEL\_S}$ | VSEL0 ~ VSEL2 Scan Interval | | | 250 | | ms |
| $T_{VSEL\_TD}$ | VSEL0 ~ VSEL2 Trap De-bounce | | | 70 | | µs |
| $I_{PSEL}$ | PSEL Current Source (Note 7) | — | | 20 | | µA |
| $I_{PSEL\_Range}$ | PSEL Current Source Range (Note 7) | — | -3 | | +3 | % |
| **GPIO SECTION** | | | | | | |
| $V_{GPIO\_HI}$ | GPIO1, GPIO4 High Voltage (Note 7) | $V_{CC}$ = 5V | 1.4 | | | V |
| $V_{GPIO\_LO}$ | GPIO1, GPIO4 Low Voltage (Note 7) | $V_{CC}$ = 5V | | | 0.4 | V |
| $I_{GPIO}$ | GPIO1, GPIO4 Sink/Source Capability (Note 7) | | 2 | | | mA |
| **PROTECTION FUNCTION SECTION** | | | | | | |
| $V_{OVP5V}$ | OVP_5V Enable Voltage (Note 6,7) | — | | 7 | | V |
| $V_{OVP20V}$ | OVP_20V Enable Voltage (Note 6,7) | — | | 22 | | V |
| $t_{DEBOUNCE\_OVP}$ | OVP De-bounce Time (Note 8) | — | — | 90 | — | ms |
| $I_{OVD}$ | Overvoltage Discharge Current | $V_{CC}$ = 5V | 150 | 200 | 250 | mA |
| $t_{OV\_DELAY}$ | Delay from OVP Threshold Trip to NMOS Gate Turn-Off (Note 7) | — | — | — | 50 | ms |

Notes: 6. 110% OVP setting @PDO>18V. PDO+2V OVP setting @PDO<=18V.
7. Guaranteed by design
8. OVP blanking time during $V_O$ transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.

## Performance Characteristics

### Function Description

The CY2569, an USB Type-C power delivery Sink controller, meets USB Power Delivery specification rev 3.0 v1.2 (USB-IF certificated TID: 5000). It provides cost effective solution without the need of external discrete high voltage components like LDOs. During the protocol handshake process, packets are transmitted and received through the embedded BMC (Biphase Mark Coding) transceiver with good eye diagram and high noise immunity. Also, the OTP ROM is used to store main protocol, application firmware and system configuration parameters. The desired PDO for the CY2569-embedded TCD could be specified through a resistor setting scheme.

### CC interface and BMC Transceiver

For the inter-operability consideration, CC interface detection and the BMC transceiver of CC are optimally designed to maintain its operating voltage tolerance and noise immunity.

### USB Power Delivery Controller

To be in full compliant with the critical USB Power Delivery specification rev 3.0 v1.2, the CY2569 is implemented through the combination of hardware and OTP firmware, to leverage the quick response time in hardware and the flexibility in software.

### Sink Voltage Selection

The CY2569 provide search algorithm for voltage request through High/Low voltage setting at VSEL0, VSEL1, and VSEL2 pins. While latches the pin setting at power on, the CY2569 also auto-scans and latches the pin setting periodically. Both fixed PDO and PPS APDO in PD source adapter are supported in CY2569 voltage search algorithm. With the 3-resistor-setting combination, the design could use the CY2569 to specify up to 8 voltage levels to fit the needs for a specific TCD.

### Power Capability Selection

With a small constant current source outputs from PSEL pin, the CY2569 measures the voltage level at the PSEL pin with the attached resistor through internal ADC. Up to 10 Power selections are supported. The designers for TCDs are recommended to use the resistor with ±1% accuracy to connect to the PSEL pin to ensure request power selection.

### NMOS VBUS Switch Control

Once the PDO negotiations are successful both in voltage selection and power selection, PWR_EN will enable NMOS VBUS switch. Any mismatch in voltage selection or power selection, NMOS VBUS switch is not turned on.

### LED Indication

GPIO4 is used to control a LED flickering, and user can learn the system status according to the LED flashing pattern which is defined in the below Table-1. Any non-PD power source is not supported in CY2569, and LED will show mismatch accordingly.

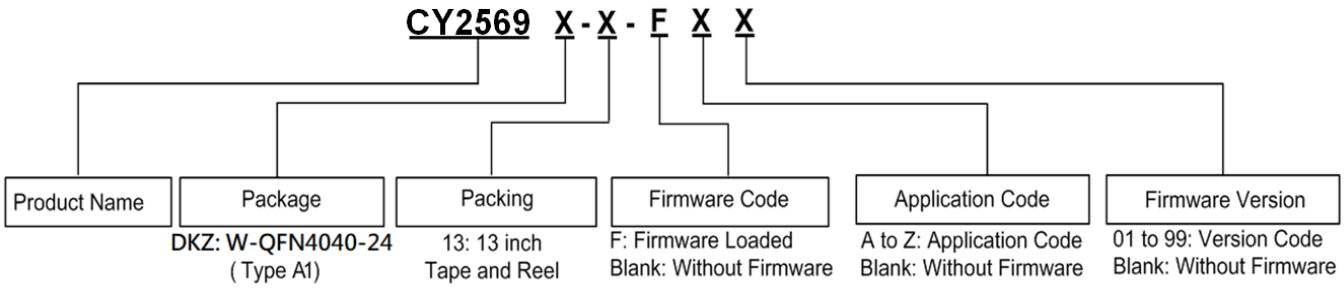
| Condition | LED Pattern | Description |
|---|---|---|
| Charging | Breathing light (2sec dimming) | 1 cycle is 4 sec |
| Fully charged | Always Light | Charging current < 500mA |
| Mismatch | 1sec Flicker | Voltage or Power Mismatch. Non-PD power source. 1 cycle is 2 sec |
| Fault | 300ms Flicker | OVP. 1 cycle is 600ms |

**Table 1 – LED Indication Table**

### OVP Protection

The CY2569 provides OVP feature by sending hard reset to the PD source when VBUS is higher than OVP voltage. Meanwhile, as soon as OVP is happened, it provides internal discharge path to reduce the overvoltage duration.

## Ordering Information




| Part Number | Package | Identification Code | 13''Tape and Reel | |
|---|---|---|---|---|
| | | | Quantity | Part Number Suffix |
| **CY2569DKZ-13** | W-QFN4040-24 (Type A1) | **CY2569** | 3000/Tape and Reel | -13 |

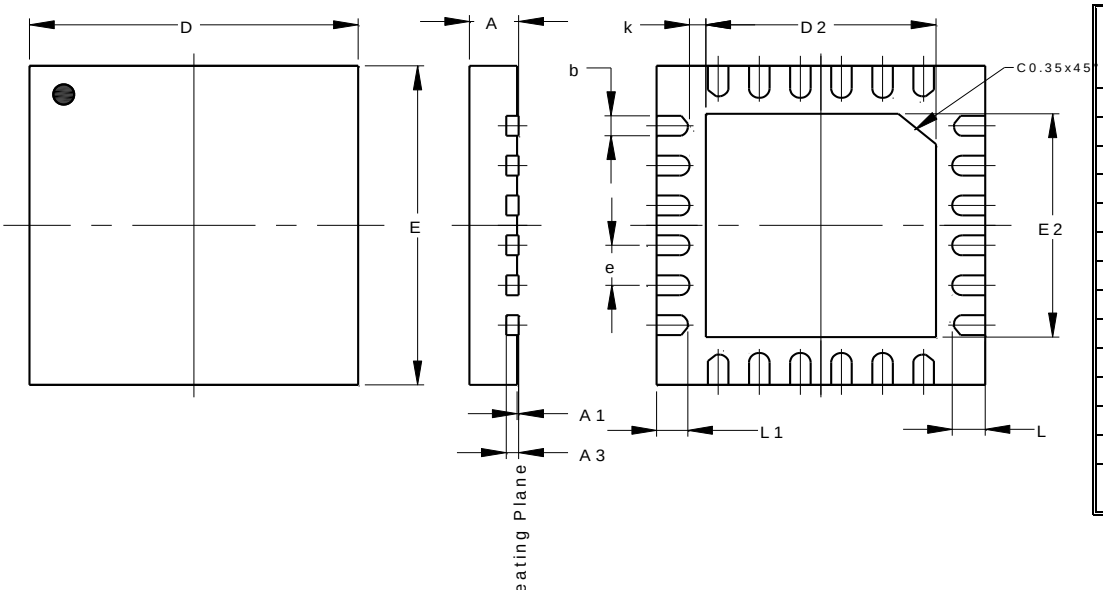
## Marking Information

**W-QFN4040-24**


| | |
|---|---|
| CY2569 | Device Name |
| YYWW | YearWeek |
| ZZ | Internal Code |

## Package Outline Dimensions

**W-QFN4040-24 (Type A1)**




| W-QFN4040-24 (Type A1) | | | |
|---|---|---|---|
| Dim | Min | Max | Typ |
| A | 0.70 | 0.80 | 0.75 |
| A1 | 0.00 | 0.05 | 0.02 |
| A3 | 0.203 REF | | |
| b | 0.20 | 0.30 | 0.25 |
| D | 4.00 BSC | | |
| D2 | 2.75 | 2.85 | 2.80 |
| E | 4.00 BSC | | |
| E2 | 2.75 | 2.85 | 2.80 |
| e | 0.50 BSC | | |
| k | 0.20 | -- | -- |
| L | 0.35 | 0.45 | 0.40 |
| L1 | 0.33 | 0.43 | 0.38 |
| All Dimensions in mm | | | |

## Suggested Pad Layout

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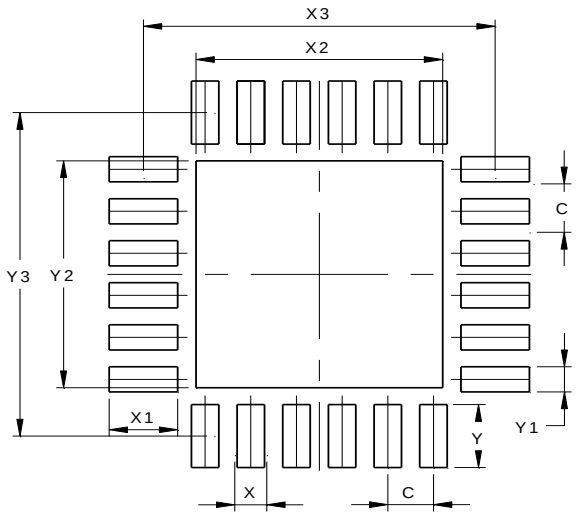
**W-QFN4040-24 (Type A1)**




| Dimensions | Value (in mm) |
|---|---|
| C | 0.500 |
| X | 0.300 |
| X1 | 0.750 |
| X2 | 2.700 |
| X3 | 3.850 |
| Y | 0.750 |
| Y1 | 0.300 |
| Y2 | 2.700 |
| Y3 | 3.850 |

## Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per J-S(e3)202
- Weight: 0.041 grams (Approximate)

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